Open-Source Chip Design: Attract More Chip Design(ers)

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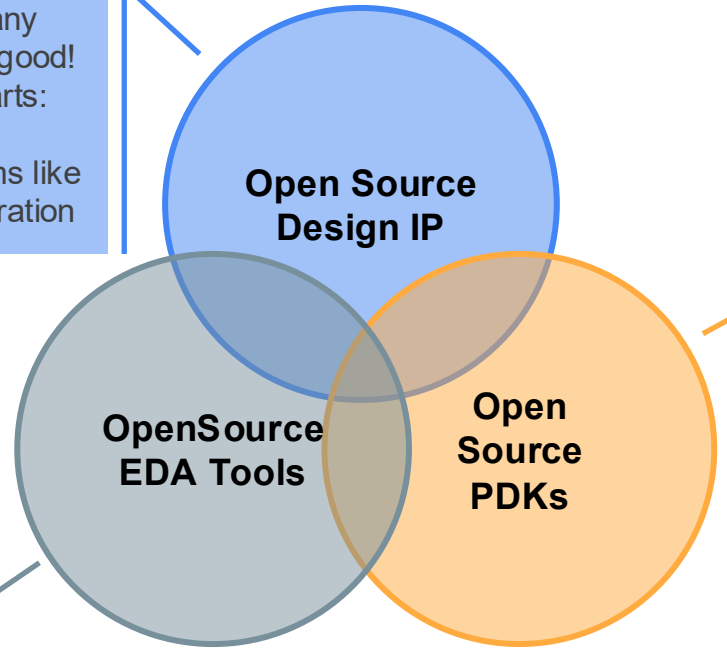
Three pillars of open-source chip design

- Reusable *building blocks* (CPU cores, peripherals, etc.), many generic IP can be common good!
- Technology-independent parts: *easy to share and reuse*
- *Widely available* on platforms like GitHub, established collaboration



- Define *properties* for a specific chip fabrication process, and not manufacturing details
- Traditionally proprietary, but some *mature nodes now open*
- Enables easy, low-barrier access to *chip manufacturing*

- *Chip design software*: design, implementation & verification
- Publicly funded projects driving *adoption* (OpenROAD, ODE4EC)
- *Common infrastructure*: build on baseline and innovate, customize into specific end-to-end flows

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Direct Impact

Enable SMEs and Newcomers

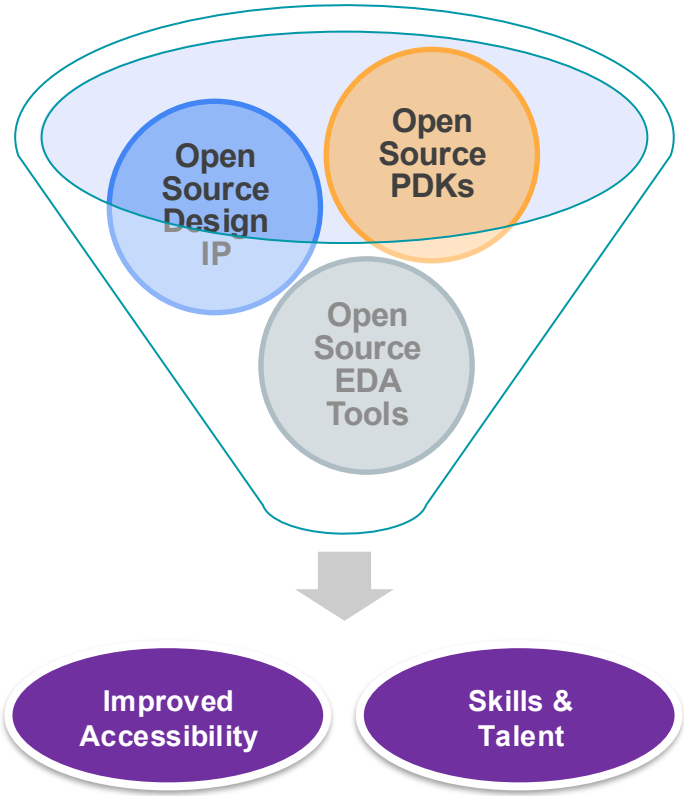
- Eliminate cost and licensing barriers
- Allow rapid prototyping and experimentation

Share and Collaborate

- Build on a shared, reusable foundation of IP
- Easily exchange and extend existing work

Nurture the Talent Pool

- Attract diverse talent with accessible tools
- Spark curiosity and hands-on learning



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Thoughts & Recommendations

- **Encourage open-source design IP**
  - Treat more reusable IP blocks (cores, interfaces, peripherals) as a *common good* that can be freely exchanged
  - Enable *rapid reuse* and innovation, accelerating research and reducing *duplicated effort*
- **Fund open-source EDA flows and point tools**
  - Invest in integrated *end-to-end flows* for frictionless chip design from RTL to GDSII
  - Support specialized point tools that *boost productivity* in verification, synthesis, and place-and-route
- **Incentivize open PDKs and open manufacturing access**
  - *Support manufacturers* in making processes openly available, new PDKs for established processes
  - An open PDK in the 65nm–28nm range would be a *game changer* for bridging research and production

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Thank you!

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